PATENT ABSTRACTS OF JAPAN

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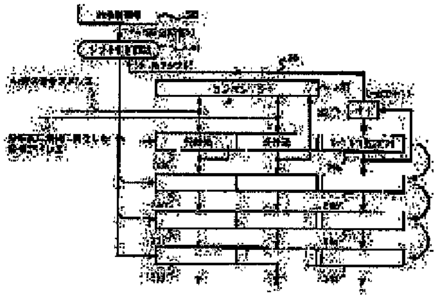
NITTA KENICHI

(54) DATA PROCESSOR

(57)Abstract:
PROBLEM TO BE SOLVED: To expand a range in which PC trace is possible for the number of PC trace register means.
SOLUTION: A data processor includes trace data registers 33a to 33d which successively store branching trace data that specify a branching origin and a branched party when a branching occurs to the instruction execution of a CPU 2, repeat number of times registers 34a to 34d, and control means 30, 31 and 32. The control means 30 to 32 have the repeat number of times registers corresponding to the branching trace data of the previous branching update the number of times data when the branching equal to the previous one occurs and obtains the trace data for another trace data register and initializes the corresponding repeat number of times register when a branching different from the previous one occurs. Even if the same branching is repeated by a repeat instruction or the like, the same trace data are blocked so that they are not stored in new trace data registers 33a to 33d.



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CLAIMS

[Claim(s)]
[Claim 1]Two or more tracing-data registers which store branching trace data for specifying an instruction address of a branching agency and a branching destination one by one when branching from which an nstruction-execution order by CPU and CPU changes occurs, Control storing of branching trace data to a repeat number of times register provided in said each tracing-data register, and said two or more tracing-data registers, and. Storing of number-of-times data to said repeat number of times register including a control means to control said control means, Number-of-times data is updated on a repeat number of times register of a tracing-data register which already has branching trace data which correspond when generating of branching is detected, and the branching is equal to the last branching, A data processor being what initializes a repeat number of times register which these branching trace data are acquired to another tracing-data register when the branching differs from the last branching, and corresponds.
[Claim 2]Two or more register means which store branching trace data for specifying an instruction address of a branching agency and a branching destination one by one when branching from which an instruction-execution

order by CPU and CPU changes occurs, Storing of branching trace data to said two or more register means including a control means to control said control means, The number of times of branching which replaces with acquisition of branching trace data new when branching trace data when branching newly arises are equal to branching trace data already stored in said register means, and relates to coincidence is stored in a corresponding register means, A data processor being what changes a register means and acquires new branching trace data when branching trace data when branching newly arises are as inharmonious as branching trace data already stored in said register means.

[Claim 3]Two or more register means which store branching trace data for specifying an instruction address of a branching agency and a branching destination one by one when branching from which an instruction-execution order by CPU and CPU changes occurs, Storing of branching trace data to said two or more register means including a control means to control said control means, The number of times of branching which replaces with acquisition of branching trace data new when branching newly arises and the branching is the repetition by execution of a repeat command, and relates to the repeat command is stored in a corresponding register means, A data processor being what changes a register means and acquires new branching trace data when branching newly arises and the branching is not the repetition by execution of a repeat command.

[Claim 4]The data processor according to claim 3, wherein said control means is what deters processing which changes a register means when branching based on interruption occurs in the middle of a repeat command, and acquires new branching trace data further.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]. Branching trace data for this invention to acquire the instruction address of a branching agency and a branching destination when branching from which an instruction-execution order by CPU (central processing unit) changes occurs can be held. It applies to the microcomputer which supports a repeat command, concerning the data processor which has what is called a PC tracing facility, and is related with effective art.

[0002]

[Description of the Prior Art]It is on board to a microcomputer and there are some which have PC tracing facility for supporting a user debugging function in it. Branching from which an instruction-execution order by CPU will change is produced with a branch instruction, interruption, exception handling, a repeat command, etc. PC tracing facility is considered as the debug support function to make the branching trace data for acquiring the instruction address of a branching agency and a branching destination hold to the register for PC trace, when said branching occurs. It has two or more sets of this PC trace register.
Whenever branching occurs, the storage location register changes one by one.

[0003]As an example of the literature in which PC tracing facility was indicated, there are the 186th page - the 188th page with a Hitachi SH7410 hardware manual of edition [2nd] (November, Heisei 9 issue), and the 195th page - the 196th page.

[0004]

[Problem(s) to be Solved by the Invention]However, in PC tracing facility of conventional technology, even if it is a case where the same branching is repeated repeatedly, since the same branching trace data are held each time, PC trace register which has a limitation in a storage capacity will be spent vainly, and PC trace cannot be performed broadly.

[0005]The purpose of this invention is to provide the data processor which can perform PC trace broadly, even if the number of register means is restricted.

[0006]The other purposes and the new feature will become clear from description and the accompanying drawing of this specification along [said] this invention.

[0007]

[Means for Solving the Problem]It will be as follows if an outline of a typical thing is briefly explained among inventions indicated in this application.

[0008]That is, a data processor is provided with the following.

CPU(2).

Two or more tracing-data registers which store branching trace data for specifying an instruction address of a branching agency and a branching destination when branching from which an instruction-execution order by CPU changes occurs one by one (33a-33d).

A repeat number of times register provided in said each tracing-data register (34a-34d).

A control means which storing of branching trace data to said two or more tracing-data registers is controlled, and controls storing of number-of-times data to said repeat number of times register (30, 31, 32, 30a, 30b).

When explaining a function of said control means comprehensively and generating of branching is detected, Number-of-times data is updated on a repeat number of times register of a tracing-data register which already has branching trace data which correspond when the branching is equal to the last branching, A repeat number of times register which these branching trace data are acquired to another tracing-data register when the branching differs from the last branching, and corresponds is initialized.

[0009]By the above, even if it is a case where the same branching is repeated by a repeat command and loop repeatedly, the situation stored in a tracing-data register with the same new tracing data each time can be prevented. Therefore, a tracing-data register for PC trace which has a limitation in a storage capacity is not spent vainly. Therefore, it becomes possible to perform PC trace broadly.

[0010]Said control means (30, 31, 32) by the 1st concrete mode, When branching trace data when branching newly arises are equal to branching trace data already stored in a register means (33a-33d and 34a-34d), Replace with acquisition of new branching trace data, and the number of times of branching concerning coincidence is stored in a corresponding register means, When branching trace data when branching newly arises are as inharmonious as branching trace data already stored in said register means, a register means is changed and new branching trace data are acquired.

[0011]Said control means (30a, 32) by the 2nd concrete mode, When branching newly arises and the branching is the repetition by execution of a repeat command, When it replaces with acquisition of new branching trace data, the number of times of branching concerning the repeat command is stored in a corresponding register means, branching newly arises and the branching is not the repetition by execution of a repeat command, a register means is changed and new branching trace data are acquired. The 2nd concrete mode is a point which deters a new tracing-data input only to a repeat command, and the circuit and function are simplified compared with the 1st concrete mode.

[0012]Said control means (30b, 32) by the 3rd concrete mode deters processing which changes a register means and acquires new branching trace data, when branching based on interruption occurs further to the 2nd concrete mode in the middle of a repeat command. According to this, even if an interrupt occurs in the middle of a repeat command, tracing data are not held by branching by the interruption. Since processing of CPU will interrupt and will return to processing at the generating time after ending interrupt processing if processing or a program is normal, if interruption in the middle of a repeat command is disregarded, the flexibility of PC trace will increase in that it becomes possible to extend the range of PC trace further.

0013]

Embodiment of the Invention]The block diagram of the microcomputer which is an example of the data processor concerning this invention is shown in drawing 6. The microcomputer 1 shown in the figure is formed in one semiconductor substrate (semiconductor chip) like single crystal silicon, for example by publicly known ntegrated circuit production technology. Although this microcomputer 1 in particular is not restricted, it has nternal bus I-Bus and peripheral bus P-Bus. These buses are provided with data, an address, and each signal wire group of a control signal.

0014]The central processing unit (CPU) 2, the user break controller (UBC) 4, X memory 5 and the Y memory 6, and the bus state controller (BSC) 7 are combined with internal bus I-Bus. The bus state controller (BSC) 7 is connected to peripheral bus P-Bus. Although not restricted to peripheral bus P-Bus in particular, An interrupt controller. (INTC) 10 A direct memory access controller. (DMAC) 11, the freerunning timer (FRT) 12, the serial communication interface (SCI) 13, the serial interface (SIO) 14, the user debugging interface 15, and the system controller 16 are combined. It is an input/output port circuit which is shown by 17 and 18 in drawing 6. The nput/output port circuit 17 interfaces with an external address bus, a data bus, and a control bus. Let the nput/output port circuit 18 be an external interface circuit for a peripheral circuit.

0015]Although especially said CPU2 is not restricted, it is provided with DSP unit 21 which has a product sum operation machine etc. with the integer units 20 which have an arithmetic logic operation machine etc. The DSP register 22 is assigned to DSP unit 21, and the general register 23 is assigned to the integer units 20. In addition, the control register 24 is formed in CPU2. The instruction controlling part 25 performs instruction control, such as an instruction fetch in CPU2, and command decoding. Based on the control signal outputted from an instruction controlling part, the data control parts 26 perform a data fetch required for an operation. CPU2 performs data processing according to the command concerned using the integer units 20 or DSP unit 21 by fetching a command from the external memory etc. which omit a graphic display, and decoding the command in the instruction decoder of the instruction controlling part 25.

[0016]In consideration of the product sum operation by said DSP unit 21, said X memory 5 and the Y memory 6 have a data path connected to CPU2 via bus X-Bus of its exclusive use, and Y-Bus.

[0017]According to the accessing object circuit (address area made into an accessing object) by CPU2 or DMAC11, said bus state controller 7 performs insertion control of access data size, access time, and the weight State, etc., and controls a bus cycle.

[0018]Synchronous operation of the above-mentioned microcomputer 1 is carried out to the clock signal outputted from the system controller 16. The interrupt controller 10 performs the mask processing and mediation to the interrupt request from the inside and outside of the microcomputer 1, or an exception-handling demand.

[0019]Although the microcomputer 1 is not a microcomputer but what is called a real chip only for evaluation, it has realized a certain amount of debugging function with the user break controller 4 and the user debugging interface 15.

[0020]When break conditions, such as an instruction address, are set up, said user break controller 4 supervises formation of the set-up break conditions and formation is detected, execution of the user program by CPU2 is suspended. The execution stops of a user program use break interruption etc. Although setting out in particular of break conditions is not restricted, it is performed via BSC7 and DMAC11 from said input/output port circuits 17 and 18.

[0021]When branching generates the user break controller 4 in the executive instruction of CPU2 by the branch instruction execution and interruption generating by CPU2, It has PC tracing facility which detects this and generates the data (branching trace data) which can specify a branch destination address and a branch source address and whose output is enabled outside. The output of branching trace data is performed from said input/output port circuits 17 and 18 using BSC7 and DMAC11.

[0022]The 1st example of PC trace circuit for realizing said PC tracing facility is shown in drawing 1. PC trace circuit is constituted by the shift control circuit 30, the comparator 31, the incrementor 32, the tracing-data registers 33a-33d, and the repeat numbers of times register 34a-34d in the figure.

[0023]Branching from which an instruction-execution order by CPU2 will change is produced with a branch instruction, interruption, exception handling, a repeat command, etc. A repeat command has a command start address, a command end address, and a repeat count as an operand. If a repeat command is executed, only said repeat count will repeat the processing which branches an executive instruction to a command start address, and executes a command to a command end address. Such a repeat command can increase the efficiency of a repetition of the product sum operation processing used abundantly by digital signal processing. Said instruction controlling part 25 asserts the branch signal 35, when said branching occurs. Namely, when a branching destination instruction address is outputted in a branch instruction or a branching destination instruction is fetched, When the leading instruction address of the manipulation routine directed by interruption is outputted in interruption or the leading instruction concerned is fetched, When said command start address is outputted in a repeat command or the start command concerned is fetched, the branch signal 35 is asserted.

[0024]Said tracing-data registers 33a-33d are registers which store the branching trace data for specifying each instruction address of branching destination and branching origin one by one, when branching from which an instruction-execution order by CPU2 changes occurs, and they have the shift register form of four steps of series. Let branching trace data be the instruction address performed at a branching destination instruction address and the last before branching in the example of drawing 1. Said repeat numbers of times register 34a-34d are formed corresponding to said each tracing-data register 33a-33d, and have the shift register form of four steps of series similarly. Although the instruction address in particular performed at said branching destination instruction address and the last before branching is not restricted, it is outputted from the instruction controlling part 25.

[0025]Said shift control circuit 30 performs shift control to the repeat numbers of times register 34a-34d and the tracing-data registers 33a-33d of shift register form. Said comparator 31 compares the information and branching destination instruction address of a branching destination which are stored in the tracing-data register 33a, and compares the information on the branching origin which may be stored in the tracing-data register 33a with the instruction address performed at the last before said branching. The state where the comparison result of the both sides by the comparator 31 is inharmonious means that branching generated immediately before is not repeated. The state of coincidence of the comparison result of the both sides by the comparator 31 means that branching generated immediately before is repeated again. As a case of the latter, there is generating of the loop by a branch instruction or repetitive operation of the 2nd henceforth [according to / a repeat command]. In the case of the former, the shift control circuit 30 performs a tracing-data registers [33a-33d] shift action with the signal 36, and new tracing data are stored in the first rank. The shift action by the shift control circuit 30 is made to deter with the signal 36 in the case of the latter, instead the value of the first rank repeat number of times register 34a is carried out +1 via the incrementor 32.

[0026]The flow chart of the control action by PC trace circuit shown in drawing 1 is shown in drawing 2. The shift control circuit 30 monitors the instruction controlling part 25 (S1), and it is judged whether the branch signal 35 was asserted (S2). Assertion of the branch signal 35 will perform the judgment of a matching state for the comparison result by the judgment 31 of a repeat, i.e., a comparator, (S3). In not being a repeat, it shifts the tracing-data registers 33a-33d and the repeat numbers of times register 34a-34d (S5). The instruction address performed at the branching destination instruction address at that time and the last before branching is stored in the register 33a, and a repeat number of times register is reset to 0 (S6). On the other hand, when the decision result of Step S3 is a repeat, said step S5 and the tracing data based on S6 are not updated, but the value of the repeat number of times register 34a is carried out +1.

[0027]Thereby, even if it is a case where the same branching is repeated by a repeat command and the loop repeatedly, the situation stored in a tracing-data register with the same new tracing data each time can be prevented. Therefore, the tracing-data register for PC trace which has a limitation in a storage capacity is not spent vainly. Therefore, it becomes possible to perform PC trace broadly. In the case of the comparative example temporarily illustrated by drawing 7, since the storage location register changes one by one whenever branching occurs, even if it is a case where the same branching is repeated repeatedly, the same branching trace data are held each time. This will spend vainly the register for PC trace which has a limitation in a storage capacity.

[0028]The 2nd example of PC trace circuit for realizing said PC tracing facility is shown in drawing 3. In the figure, the shift control circuit 30a where the comparator 31 is excluded to drawing 1, instead PC trace circuit receives the repeat execution signal 37 is formed. Other composition is the same as drawing 1. Said repeat execution signal 37 is asserted when branching in a repeat command is repeated. If it puts in another way, when a repetition of processing by repeat command is performed, the repeat execution signal 37 will be asserted. When the repeat execution signal 37 is asserted, the branch signal 35 is certainly asserted. If the repeat execution signal 37 is asserted, the shift control circuit 30a will deter the shift action to the tracing-data registers 33a-33d and the repeat numbers of times register 34a-34d, even if the branch signal 35 is asserted. It replaces with it and the value of the repeat number of times register 34a is carried out +1 using an incrementor.

[0029]Thus, PC trace circuit of drawing 3 is a point which deters a data registers [33a-33d and 34a-34d] shift action only to a repeat command although circuitry is easy compared with drawing 1, and the function is simplified compared with drawing 1. In respect of others, it has the same effect as drawing 1.

[0030]The 3rd example of PC trace circuit for realizing said PC tracing facility is shown in drawing 4. In the figure, the shift control circuit 30b is [PC trace circuit] different to drawing 3. The status signal 38a and the nterrupt signal 38b which show a certain thing in the middle of are supplied to the shift control circuit 30b to the composition of drawing 3. [the repeat command] Said status signal 38a is asserted when the instruction controlling part 25 decodes the instruction code of a repeat command, and it is negated by ending processing for the repeat count specified with a repeat command. according to the state where the status signal 38a is asserted, branching in a repeat instruction execution or a repeat instruction execution has produced the shift control circuit 30b — if it puts in another way, a certain thing can be recognized in the middle of a repeat command. the renewal of data of as opposed to [when recognizing the shift control circuit 30b a certain thing in the middle of a repeat command with said status signal 38a, even if branching based on interruption generates] the tracing-data register 33a, the registers 33a-33d, and 34a-34d — shift action deterrence is carried out. Generating of branching based on interruption is recognized by assertion of the branch signal 35 and the nterrupt signal 38b.

[0031]Therefore, even if an interrupt occurs in the middle of a repeat command in the composition of drawing 4, tracing data are not held in branching by the interruption. Since processing of CPU will interrupt and will return to the processing at the generating time after interrupt processing is completed if processing or a program is normal, if convenient even if such interruption processing is disregarded, the demand of extending the range of PC trace further can be coped with, and flexibility can be increased.

[0032]The 4th example of PC trace circuit for realizing said PC tracing facility is shown in drawing 5. In the igure, the flags 40a-40d are set as the shift control target by the shift control circuit 30c. The instruction address performed at a branching destination instruction address and the last before branching is supplied to the tracing-data registers 33a-33d via the input gates 42a-42d. a repeat numbers of times register [34a-34d] value — the incrementor 41 — it is made alternative by a-41 d +1. The +1 operation by the incrementors 41a-41d is controlled by assertion of the repeat execution signal 37. It is controlled by a flags [40a-40d] value which input gates 42a-42d which incrementors 41a-41d are operated, and are operated. The flags 40a-40d are shifted by the shift control circuit 30c, when branching arises with the branch signal 35 and it is not the repetition by repeat command. Therefore, even if it is not the shift register form which connected the above-mentioned tracing-data register in in-series, the same effect as drawing 1 can be acquired.

[0033]Although the invention made by this invention person above was concretely explained based on the embodiment, it cannot be overemphasized that it can change variously in the range which this invention is not limited to it and does not deviate from the gist.
[0034]For example, the number of stages of a tracing-data register is not limited to four steps, but can be changed suitably. The functional real module of a microcomputer is not limited to drawing 6. The circuit block which supports PC tracing facility is not limited to a user break controller, either.
[0035]Although the above explanation explained the case where it applied to the microcomputer which has a DSP unit which is the field of the invention which became the background about the invention mainly made by this invention person, This invention is not limited to it but can apply CPU to the data processor which executes a hidden command or a command widely.
[0036]
[Effect of the Invention]It will be as follows if the effect acquired by the typical thing among the inventions indicated in this application is explained briefly.
[0037]That is, even if it is a case where the same branching is repeated by a repeat command and the loop repeatedly, the situation stored in a tracing-data register with the same new tracing data each time can be prevented. Therefore, the tracing-data register for PC trace which has a limitation in a storage capacity is not spent vainly. Therefore, it becomes possible to perform PC trace broadly.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing the 1st example of PC trace circuit for realizing PC tracing facility.
[Drawing 2]It is a flow chart which shows an example of the control action by PC trace circuit shown in drawing 1.
[Drawing 3]It is a block diagram showing the 2nd example of PC trace circuit for realizing PC tracing facility.
[Drawing 4]It is a block diagram showing the 3rd example of PC trace circuit for realizing PC tracing facility.
[Drawing 5]It is a block diagram showing the 4th example of PC trace circuit for realizing PC tracing facility.
[Drawing 6]It is a block diagram, showing the microcomputer which is an example of the data processor concerning this invention on the whole.
[Drawing 7]It is a block diagram showing PC trace circuit of the form which updates tracing data each time whenever branching occurs as a comparative example.
[Description of Notations]
1 Microcomputer
2 CPU
4 User break controller
25 Instruction controlling part
30, 30a, 30b, 30c shift control circuit
31 Comparator
32 Incrementor
33a-33d Tracing-data register
34a-34d repeat number of times register
35 Branch signal
37 Repeat execution signal
38a The status signal which shows a certain thing in the middle of a repeat command
38b Interrupt signal
40a-40d Flag
41a-41d Incrementor

42a-42d input gate

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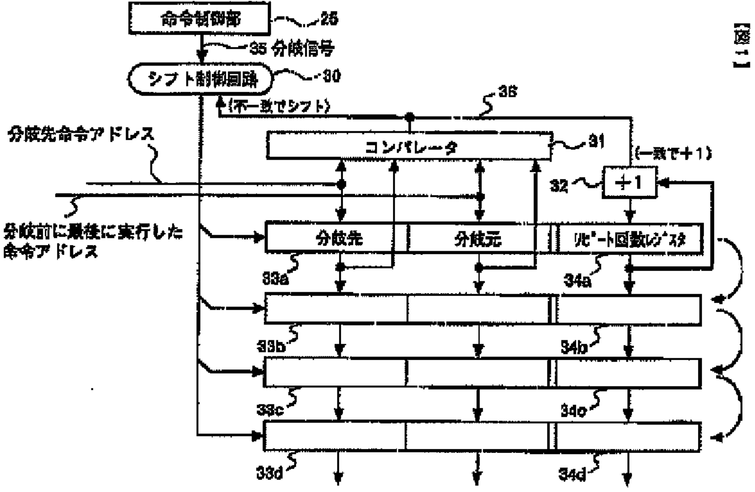
DRAWINGS

[Drawing 1]


命令制御部
25
35 分岐信号
シフト制御回路
30
(不一致でシフト)
36
分岐先命令アドレス
コンパレータ
31
(一致で+1)
32
+1
分岐前に最後に実行した命令アドレス
分岐先
分岐元
リピート回数レジスタ
33a
34a
33b
34b
33c
34c
33d
34d
【図1】

[Drawing 2]

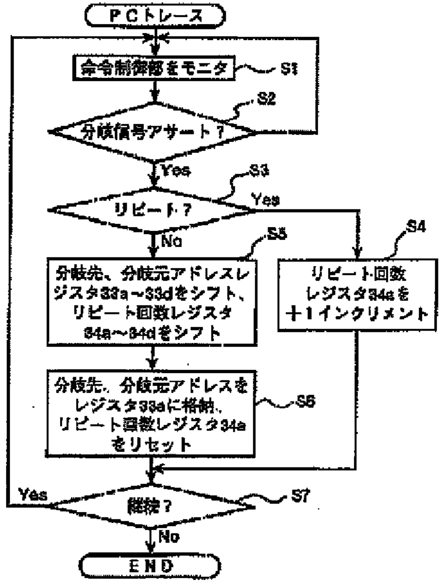
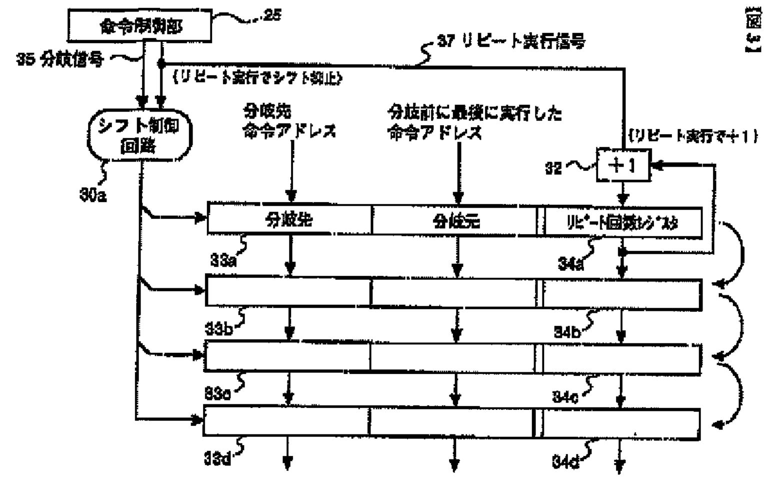


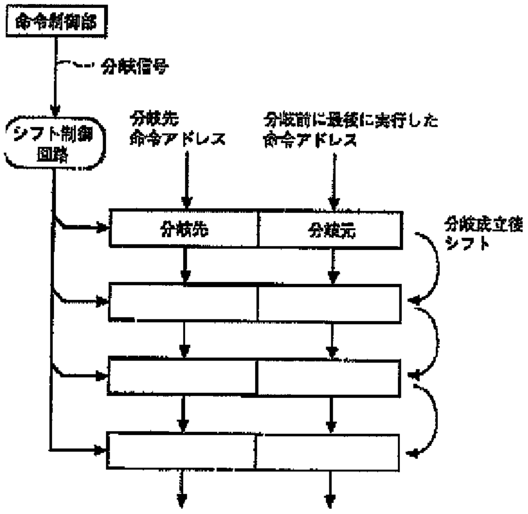
図2】
PCトレース
命令制御部をモニタ
S1
S2
分岐信号アサート？
Yes
S3
リピート？
Yes
No
S5
S4
分岐先、分岐元アドレスレジスタ33a～33dをシフト、リピート回数レジスタ34a～34dをシフト
リピート回数レジスタ34aを+1インクリメント
分岐先、分岐元アドレスをレジスタ33aに格納、リピート回数レジスタ34aをリセット
S6
Yes
継続？
S7
No
END

[Drawing 3]

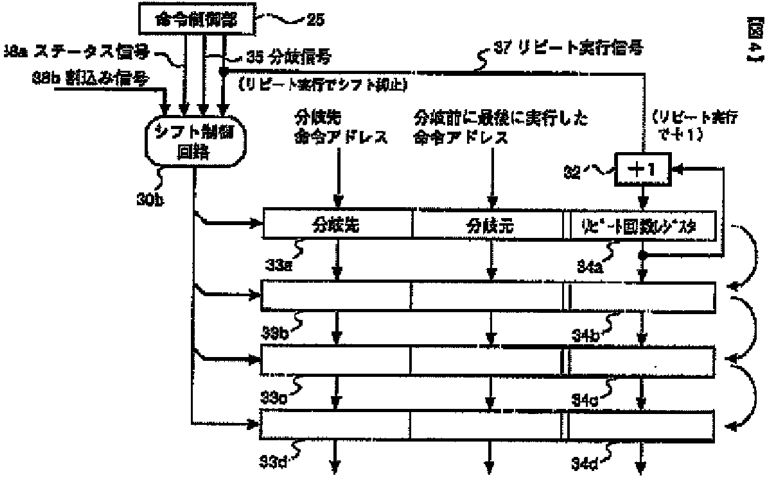

【図3】
命令制御部
25
35 分岐信号
37 リピート実行信号
（リピート実行でシフト抑止）
シフト制御回路
30a
分岐先命令アドレス
分岐前に最後に実行した命令アドレス
（リピート実行で＋1）
32
＋1
分岐先
分岐元
リピート回数レジスタ
33a
34a
33b
34b
33c
34c
33d
34d

[Drawing 7]

【図7】

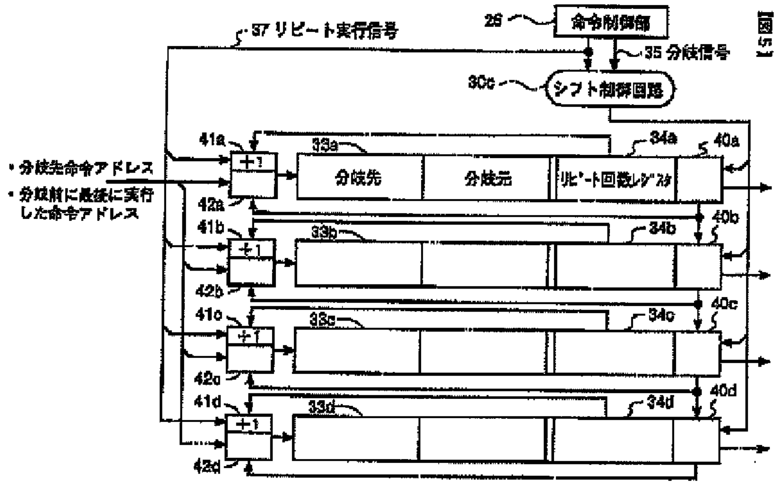

命令制御部
分岐信号
シフト制御回路
分岐先命令アドレス
分岐前に最後に実行した命令アドレス
分岐先
分岐元
分岐成立後シフト

[Drawing 4]

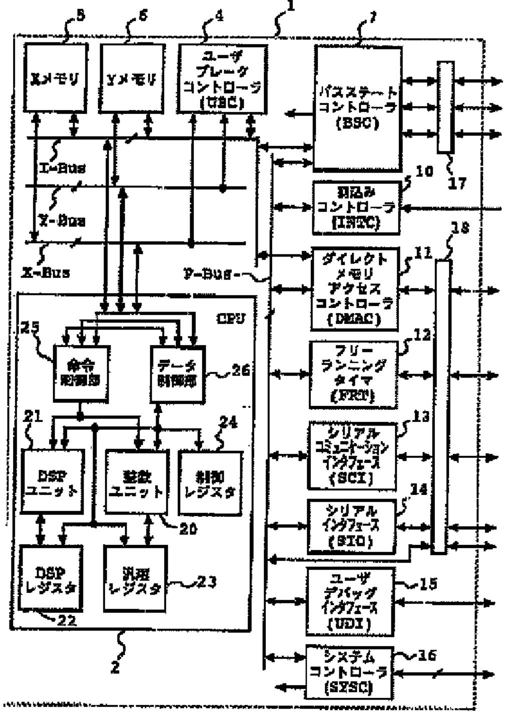

【図4】
命令制御部
25
8a ステータス信号
38b 割込み信号
35 分岐信号
37 リピート実行信号
（リピート実行でシフト抑止）
シフト制御回路
30b
分岐先命令アドレス
分岐前に最後に実行した命令アドレス
（リピート実行で＋1）
32
＋1
分岐先
分岐元
リピート回数レジスタ
33a
34a
33b
34b
33c
34c
33d
34d

[Drawing 5]

【図5】


26 命令制御部
37 リピート実行信号
35 分岐信号
30c シフト制御回路
41a
33a
34a
40a
・分岐先命令アドレス
・分岐前に最後に実行した命令アドレス
+1
分岐先
分岐元
リピート回数レジスタ
42a
41b
33b
34b
40b
42b
41c
33c
34c
40c
42c
41d
33d
34d
40d
42d

[Drawing 6]
【図6】


5
6
4
1
7
Xメモリ
Yメモリ
ユーザブレークコントローラ(UBC)
バスステートコントローラ(BSC)
17
I-Bus
Y-Bus
X-Bus
P-Bus
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[Translation done.]